IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/618,237
Applicant	:	Gang Zhang et al.
Filed	:	July 11, 2003
Title	:	ANALOG INTEGRATED CIRCUIT LAYOUT DESIGN
Group Art Unit	:	2825
Examiner	:	Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the requirements of 37 C.F.R. §§1.56, 1.97 and 1.98, Applicants submit this Information Disclosure Statement together with completed Form(s) PTO/SB/08A and a copy of each reference listed thereon.

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Deborah L. Medves
(Name of Person Mailing Papers)

Deborah L. Medves 12/30/03
Signature Date

this Information Disclosure Statement are enclosed.

Respectfully submitted,

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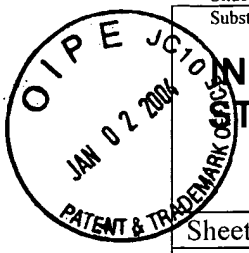

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Attorney Docket Number	2879-030687

Sheet 1 of 3

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, cite and/or country where published.	T[2]
	1	R. HARJANI, R.A. RUTENBAR and L.R. CARLEY, "OASYS: A Framework For Analog Circuit Synthesis", IEEE Transactions On Computer-Aided Design, Vol. 8, No. 12, pp. 1247-1266, (December 1989).	
	2	M.G.R. DEGRAUWE, O. NYS, E. DIJKSTRA, J. RIJMENANTS, S. BITZ, B.L.A.G. GOFFART, E.A. VITTOZ, S. CSERVENY, C. MEIXENBERGER, G. VAN DER STAPPEN, and H. J. OGUEY, "IDAC: An Interactive Design Tool For Analog CMOS Circuits", IEEE Journal Of Solid State Circuits, Vol. Sc-22, No. 6, pp. 1106-1116, (December 1987).	
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	4	E. OCHOTTA, L.R. CARLEY and R.A. RUTENBAR, "Analog Circuit Synthesis For Large, Realistic Cells: Designing A Pipelined A/D Converter With ASTRX/OBLX", in Proc., IEEE Custom Integrated Circuit Conference, pp. 365-368, (1994).	
	5	R. PHELPS, M. KRASNICKI, R.A. RUTENBAR, L.R. CARLEY and J.R. HELLUMS, "A Case Study Of Synthesis For Industrial-Scale Analog IP: Redesign Of The Equalizer/Filter Frontend For An ADSL CODEC", ACM/IEEE Design Automation Conference, pp. 1-6 (June 2000).	
	6	G.G.E. GIELEN and R.A. RUTENBAR, "Computer-Aided Design Of Analog And Mixed-Signal Integrated Circuits", Proceedings Of The IEEE, Vol. 88, No.12, pp. 1825-1852 (December 2000).	
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	8	E. FELT, E. MALAVASI, E. CHARBON, R. TOTARO and A. SANGIOVANNI-VINCENTELLI, "Performance-Driven Compaction For Analog Integrated Circuits", IEEE 1993 Custom Integrated Circuits Conference, pp. 17.3.1-17.3.5, (1993).	
	9	U. CHOUDHURY and A. SANGIOVANNI-VICENTELLI, "Constraint Generation For Routing Analog Circuits", 27th ACM/IEEE Design Automation Conference, pp. 561-566, (June 1990).	
	10	E. CHARBON, E. MALAVASI, U. CHOUDHURY, A. CASOTTO and A. SANGIOVANNI-VICENTELLI, "A Constraint-Driven Placement Methodology For Analog Integrated Circuits", IEEE 1992 Custom Integrated Circuits Conference, pp. 28.2.1-28.2.4, (May 1992).	

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	11	E. CHARBON, E. MALAVASI, D. PANDINI and A. SANGIOVANNI-VINCENTELLI, "Imposing Tight Specifications On Analog IC's Through Simultaneous Placement And Module Optimization", IEEE 1994 Custom Integrated Circuits Conference, pp. 525-528, (May 1994).	
	12	E. CHARBON, G. HOLMLUND, A. SANGIOVANNI-VICENTELLI and B. DONECKER, "A Performance-Driven Router For RF And Microwave Analog Circuit Design", IEEE 1995 Custom Integrated Circuits Conference, pp. 383-386, (May 1995).	
	13	E. MALAVASI and A. SANGIOVANNI-VICENTELLI, "Area Routing For Analog Layout", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 12, No. 8, pp. 1186-1197, (August 1993).	
	14	E. MALAVASI and A. SANGIOVANNI-VICENTELLI, "Dynamic Bound Generation For Constraint-Driven Routing", IEEE 1995 Custom Integrated Circuits Conference, pp. 477-480, (May 1995).	
	15	P. VANCORENLAND, G. VAN DER PLAS, M. STEYAERT, G. GIELEN, and W. SANSEN, "A Layout-Aware Synthesis Methodology For RF Circuits", 2001 IEEE, pp. 358-362, (2001).	
	16	K. LAMPAERT, G. GIELEN and W. SANSEN, "Direct Performance-Driven Placement Of Mismatch-sensitive Analog Circuits", 32nd ACM/IEEE Design Automation Conference, pp. 445-449, (June 1995).	
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	18	J.M. COHEN, D.J. GARROD, R.A. RUTENBAR and L.R. CARLEY, "KOAN/ANAGRAM II: New Tools For Device-Level Analog Placement And Routing", IEEE Journal Of Solid-State Circuits, Vol. 26, No. 3, pp. 330-342, (March 1991).	
	19	S. MITRA, S.K. NAG, R.A. RUTENBAR and L.R. CARLEY, "System-Level Routing Of Mixed-Signal ASICs IN WREN", Proc. IEEE Conference On Computer Aided Design, pp. 394-399, (November 1992).	
	20	S. MITRA, R.A. RUTENBAR, L.R. CARLEY and D. J. ALLSTOT, "Substrate-Aware Mixed-Signal Macro-Cell Placement In WRIGHT", IEEE Journal Of Solid-State Circuits, Vol. 30, No. 3, pp. 269-278, (March 1995).	

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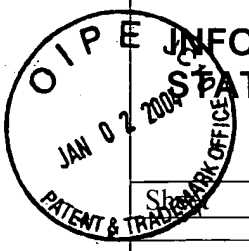

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	21	G. ZHANG, A. DENGI, and L.R. CARLEY, "Automatic Synthesis Of A 2.1GHz SiGe Low Noise Amplifier", IEEE RFIC Symposium, pp. 1-4 (June 2002).	

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